Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

Claims 1-21 (canceled)

22. (new) A phase-locked loop circuitry, comprising:

a comparator configured to compare phases of a reference clock signal and an output signal of said apparatus and to output a voltage in accordance with a difference in phase as a comparison result;

a filter configured to integrate the voltage output from said comparator;

a voltage-controlled oscillator configured to control a frequency of an output signal in accordance with the voltage output from said filter, said voltage-controlled oscillator comprising:

a ring oscillator configured to include a delay circuit including a plurality of inverters connected in a ring form;

a plurality of first transistors corresponding to said plurality of inverters of said ring oscillator on a one-to-one basis and configured to control a current supplied by a first power source voltage to a positive side power source terminal of each of said plurality of inverters;

a plurality of second transistors corresponding to said plurality of inverters of said ring oscillator on a one-to-one basis and configured to control a current output from a negative side power source terminal of each of said plurality of inverters;

a voltage-to-current converter configured to convert said voltage output from said filter into a current; and

a plurality of current mirror circuits configured to output currents in accordance with the current output from said voltage-to-current converter to a control signal input terminal of each said plurality of first transistors and to a control signal input terminal of each of said plurality of second transistors;

wherein a portion of said voltage-controlled oscillator including said ring oscillator operates with a first power source voltage, and another portion of said voltage-controlled oscillator including said voltage-to-current converter operates with a second power source voltage greater than said first power source voltage.

23. (new) A phase-locked loop circuitry as defined in claim 22, wherein said current mirror circuit comprises:

a first current mirror circuit configured to output a current in accordance with the current output from said voltage-to-current converter;

a second current mirror circuit configured to output a current in accordance with the current output from said first current mirror circuit to a control signal input terminal of each of said plurality of first transistors; and

a third current mirror circuit configured to output a current in accordance with the current output from said second current mirror circuit to a control signal input terminal of each of said plurality of second transistors.

24. (new) A phase-locked loop circuitry as defined in claim 23, wherein said first and second current mirror circuits operate with said second power source voltage, and said third current mirror circuit operates with said first power source voltage.

25. (new) A phase-locked loop circuitry as defined in claim 23, wherein said voltage-to-current converter includes a constant current source configured to supply a predetermined constant current to said first current mirror circuit.

26. (new) A phase-locked loop circuitry as defined in claim 23, wherein said third current mirror circuit includes a transistor with which each of said plurality of first transistors forms a current mirror circuit.

27. (new) A phase-locked loop circuitry as defined in claim 23, wherein said voltage-to-current converter includes a transistor configured to form a current mirror circuit with each of said plurality of second transistors and to receive a current output from said third current mirror circuit.

28. (new) A phase-locked loop circuitry, comprising:

a comparator configured to compare phases of a reference clock signal and an output signal of said apparatus and to output a voltage in accordance with a difference in phase as a comparison result;

a filter configured to integrate the voltage output from said comparator;

a voltage-controlled oscillator configured to control a frequency of an output signal in accordance with the voltage output from said filter, said voltage-controlled oscillator comprising:

a ring oscillator configured to include a delay circuit including a plurality of differential amplifiers connected in a ring form, each of said plurality of differential amplifier including a first transistor for controlling a current supplied to a corresponding one of said plurality of differential amplifiers by a first power source voltage and a second transistor for controlling a current output from a corresponding one of said plurality of differential amplifiers;

a voltage-to-current converter configured to convert said voltage output from said filter into a current; and

a plurality of current mirror circuits configured to output currents in accordance with the current output from said voltage-to-current converter to a control signal input terminal of each of said plurality of first transistor and to a control signal input terminal of each of said plurality of second transistors;

wherein a portion of said voltage-controlled oscillator including said ring oscillator operates with a first power source voltage, and another portion of said voltage-controlled oscillator including said voltage-to-current converter operates with a second power source voltage greater than said first power source voltage.

29. (new) A phase-locked loop circuitry as defined in claim 28, wherein said current

mirror circuit comprises:

a first current mirror circuit configured to output a current in accordance with the current output from said voltage-to-current converter;

a second current mirror circuit configured to output a current in accordance with the current output from said first current mirror circuit to a control signal input terminal of said first transistor; and

a third current mirror circuit configured to output a current in accordance with the current output from said second current mirror circuit to a control signal input terminal of said second transistor.

30. (new) A phase-locked loop circuitry as defined in claim 29, wherein said first and second current mirror circuits operate with said second power source voltage, and said third current mirror circuit operates with said first power source voltage.

31. (new) A phase-locked loop circuitry as defined in claim 29, wherein said voltage-to-current converter includes a constant current source configured to supply a predetermined constant current to said first current mirror circuit.

32. (new) A phase-locked loop circuitry as defined in claim 29, wherein said third current mirror circuit includes a transistor with which said first transistor forms a current mirror circuit.

33. (new) A phase-locked loop circuitry as defined in claim 29, wherein said voltage-to-current converter includes a transistor configured to form a current mirror circuit with said second transistor and to receive a current output from said third current mirror circuit.

34. (new) A method of phase-locked looping, comprising the steps of:

providing step providing a ring oscillator including a plurality of inverters connected in a ring form;

comparing step comparing phases of a reference clock signal and an output signal of said ring oscillator;

generating step generating a voltage in accordance with a difference in phase as a comparison result;

integrating step integrating the voltage output from said generating step;

converting step converting said voltage output from said integrating step into a current;

a plurality of mirroring steps mirroring said current converted in said converting step to output first and second currents in accordance with the current output from said converting step;

first applying step applying said first current output in said mirroring steps to a plurality of first transistors corresponding to said plurality of inverters of said ring oscillator on a one-to-one basis to control a current supplied by a first power source voltage to a positive side power source terminal of each of said plurality of inverters; and

second applying step applying said second current output in said mirroring steps to a plurality of second transistors corresponding to said plurality of inverters of said ring oscillator on a one-to-one basis to control a current output from a negative side power source terminal of each of said plurality of inverters,

wherein said converting step operates with a second power source voltage greater than the first power source voltage, and said ring oscillator operates with said first power source voltage.

35. (new) A method of phase locked looping, comprising the steps of:

providing step providing a ring oscillator including a plurality of differential amplifiers connected in a ring form, each of said plurality of differential amplifiers including first and second transistors;

comparing step comparing phases of a reference clock signal and an output signal of said ring oscillator;

generating step generating a voltage in accordance with a difference in phase as a comparison result;

integrating step integrating the voltage output from said generating step;

converting step converting said voltage output from said integrating step into a current;

a plurality of mirroring steps mirroring said current converted in said converting step to output first and second currents in accordance with the current output from said converting step;

first applying step applying said first current output in said mirroring steps to said first transistor included in each of said plurality of differential amplifiers of said ring oscillator to control a current supplied by a first power source voltage to each of said plurality of differential amplifiers; and

second applying step applying said second current output in said mirroring steps to said second transistor included in each of said plurality of differential amplifiers of said ring oscillator to control a current output from a negative side power source terminal of each of said plurality of differential amplifiers,

wherein said converting step operates with a second power source voltage greater than the first power source voltage, and said ring oscillator operates with said first power source voltage.